Amendments to the Specification:

Please replace the paragraph on page 1, lines 7-14 with the following amended paragraph:

The invention relates to a time-division multiplex method for transmitting data bits which are allocated to a number of channels. The data bits are transmitted in accordance with a predetermined time sequence in time-division multiplex frames at a predetermined data rate on a transmission path. The frames include in each case a number of ~~multiplets~~ time slots, namely one ~~multiplet~~ time slot including a predetermined number of bits for each channel.

Please replace the paragraph on page 6, lines 5-9 with the following amended paragraph:

Generally, the data burst allocated to one channel can naturally contain another number of data bits, e.g. four or 16 bits instead of eight bits, so that generally one bit multiplet or time slot including a predetermined number of bits is allocated to each channel.

Please replace the paragraphs beginning on page 7, line 18 and ending on page 8, line 23 with the following amended paragraphs:

providing a given time sequence in time-division multiplex frames for transmitting the data bits with a given data rate on a transmission path, the time-division multiplex frames each containing a plurality of ~~multiplets~~ time slots such that for each of the channels a respective one of the ~~multiplets~~ time slots includes a given number of the data bits; and

transmitting, in the time-division multiplex frames, in accordance with a given allocation of the channels to groups each including a subset of the channels, the ~~multiplets~~ time slots of each of the groups in a time-interleaved manner such that between respective two of the data bits of one of the ~~multiplets~~ time slots of a given one of the groups there is a respective one of the data bits of each remaining one of the ~~multiplets~~ time slots of the given one of the groups and such that the groups are transmitted sequentially.

In other words, the object is achieved by a a time-division multiplex method for transmitting data bits which are allocated to a number of channels, in which method the data bits are transmitted in accordance with a predetermined time sequence in time-division multiplex frames at a predetermined data rate on a transmission path, the frames in each case containing a number of ~~multiplets~~ time slots, namely one

~~multiplet~~ time slot including a predetermined number of bits for each channel, wherein in the frames in accordance with a predetermined allocation of the channels to groups with a predetermined subset or partial number of the channels,

- the ~~multiplets~~ time slots of in each case one group are transmitted time-interleaved, namely one bit each of each of the remaining ~~multiplets~~ time slots of the group between two bits each of a ~~multiplet~~ time slot,

Please replace the paragraphs beginning on page 9, line 1 and ending on page 9, line 22 with the following amended paragraphs:

Due to this solution, the object of the invention is achieved in a simple manner. The data bits can be generated in the decentralized components at a processing rate which is below the data rate of the centralized system bus and are transmitted "interleaved" on the system bus. Due to the interleaving of the bits (or digital characters) of the ~~multiplets~~ time slots in each case in a group of channels, the data processing speed can be retained or even reduced in the decentralized components while the total data rate on a central bus system is distinctly increased. In particular, the invention makes it possible to retain the previously used

circuit technology of the decentralized components and also the architecture of the distribution system.

In accordance with another mode of the invention, a clock signal has a clock rate corresponding to the given data rate divided by a number of the channels allocated to the subset; a transmission of the data bits is clocked with the clock signal; and the clocking of the transmission of the data bits is triggered in each of the groups of successive ones of the ~~multiplets~~ time slots with a mutual offset by one clock unit corresponding to the data rate.

Please replace the paragraph on page 10, lines 6-13, with the following amended paragraph:

In accordance with a further mode of the invention, the channels are grouped in channel pairs, each of the ~~cannel~~ channel pairs including a first channel and a second channel; the data bits of associated ones of the ~~multiplets~~ time slots of the first channel in each of the groups are clocked with a first half of the clock unit; and the data bits of associated ones of the ~~multiplets~~ time slots of the second channel in each of the groups are clocked with a second half of the clock unit.

Please replace the paragraphs beginning on page 10, line 24 and ending on page 11, line 19 with the following amended paragraphs:

For the purpose of reducing electromagnetic interference radiation, it is recommended to use system clocks having low frequencies; these also allow simple or inexpensive components to be used. It is, therefore, advantageous if the transmission of the bits is clocked through the use of a clock signal, the clock rate of which corresponds to the data rate divided by the part-number of the channels in a group, but the clocking of the bits of ~~multiplets~~ time slots in each case following one another in a group is triggered with mutual offset by one clock unit corresponding to the data rate.

In a preferred embodiment of the invention which is distinguished by particular simplicity and efficiency in the evaluation of the clock signals, the channels are grouped in pairs and the clocking of the bits of one channel or, respectively, of the associated ~~multiplet~~ time slot in each group occurs via one clock half, and the clocking of the bits of the other channel or, respectively, of the associated ~~multiplet~~ time slot occurs via the other clock half of the clock signal. This can be done, in particular, in a level-controlled manner via the high phase or the low phase or edge-

controlled through the use of rising or, respectively, falling edges.

Please replace the paragraphs on page 12, lines 9-23 with the following amended paragraphs:

a plurality of latches, the latches receiving burst signals, the burst signals being allocated to groups each including a respective number of the burst signals, the burst signals containing respective data bit ~~multiplets~~ time slots within a period of time-division multiplex frames with a given data rate, each of the data bit ~~multiplets~~ time slots including a given number of data bits;

the latches being configured such that given ones of the latches allocated to one of the groups are driven in a time-shifted manner with a relative time offset with respect to one another for a time-interleaved transmission of the data bit ~~multiplets~~ time slots of the burst signals, the relative time offset of the given ones of the latches within the one of the groups being smaller than a time interval between two of the data bits of one of the ~~multiplets~~ time slots;

Please replace the paragraph on page 13, lines 4-21 with the following amended paragraph:

In other words, according to the invention, a device suitable for generating time-division multiplex signals which can be transmitted in accordance with the method according to the invention is, in particular, a device in which - on the basis of a number of burst signals which in each case contain one data bit ~~multiplet~~ time slot with a predetermined number of bits within predetermined time multiplex frames with a predetermined data rate - according to a predetermined allocation of the burst signals to groups with a predetermined part-number of burst signals,

- the burst signals are in each case supplied to a latch, the latches of in each case one group can be driven with mutual time offset for time-interleaved transmission of the ~~multiplets~~ time slots of the burst signals, the relative time offset of the latches within the relevant group being smaller than the time interval between two bits of a ~~multiplet~~ time slot, and
- the outputs of the latches are combined via a common multiplexer device.

Please replace the paragraph on page 16, lines 13-21 with the following amended paragraph:

a plurality of latches, the latches receiving a time-division multiplex signal including, within time-division multiplex frames, data bits with a given data rate, the time-division multiplex frames containing a plurality of ~~multiplets~~ time slots such that the ~~multiplets~~ time slots are provided for respective ones of a plurality of burst signals, the burst signals being allocated to groups each including a number of the burst signals, and each of the ~~multiplets~~ time slots including a given number of the data bits;

Please replace the paragraphs beginning on page 17, line 1 and ending on page 17, line 25 with the following amended paragraphs:

respective ones of the latches allocated to in each case one of the groups being driven with a mutual time offset with respect to one another such that, between driving two of the data bits of a given one of the ~~multiplets~~ time slots of a given one of the groups, one of the data bits of each remaining one of the ~~multiplets~~ time slots of the given one of the groups is driven. .

In other words, as a device for obtaining a number of burst signals from a time-division multiplex signal transmitted in accordance with a method according to the invention - which

contains data bits with a predetermined data rate in the time-division multiplex signal within predetermined time-division multiplex frames with a predetermined data rate, the frames in each case containing a number of ~~multiplets~~ time slots, namely one ~~multiplet~~ time slot with a predetermined number of bits for each burst signal - a device is particularly suitable, according to the invention, in which, according to a predetermined allocation of the burst signals to groups with a predetermined part-number of burst signals, the time-division multiplex signal is supplied to latches, one latch in each case being allocated to one burst signal, and the latches of in each case one group can be driven with mutual time offset, where one bit each of each of the remaining ~~multiplets~~ time slots of the group can be driven between the driving of respective two bits each of a ~~multiplet~~ time slot of the group.

Please replace the paragraphs beginning on page 22, line 6 and ending on page 24, line 7 with the following amended paragraphs:

In the example shown here, duplication of the clock rate ck8 of the PCM bus compared with the original clock rate ck4 achieves a doubling of the number of the useable channels so that up to 128 channels are now available. According to the

invention, the bit octets are transmitted "interleaved" in groups which is shown by way of example in Fig. 2. In the example shown here, two octets are in each case interleaved as is shown in Fig. 2 with the example of signals cha, chb of channels CHA, CHB. These two channels form a group GAB where, according to the invention, the octets of in each case one group are transmitted time-interleaved instead of by themselves and one octet after the other in a known manner, in the time-division multiplex signal pb. In this configuration, there is in each case one bit of each of the remaining ~~multiplets~~ time slots of the group - in the present example bit b7 of channel CHB between each two bits of an octet - for example between bits b7 and b6 of the channel CHA. After the transmission of the total of 2 x 8 = 16 bits of this group, the bits of the next group GCD are transmitted which, according to the invention, are formed of the interleaved octets of the channels CHC and CHD, etc. The bits in the signal ~~bp~~ pb of the PCM bus ZB are thus transmitted on the basis of the "fast" clock ck8, the data bits following one another at a clock period t8 of 122 ns. In contrast, the data processing in the SLM cards takes place on the basis of the "slow" clock ck4 or, respectively, a clock ck4' derived therefrom, which is why the validity period of the bits of the transmitting parts SXA,..., SXN and of the receiving parts

SRA,..., SRN of the SLM cards corresponds to the bit period t4 of this latter clock, thus 244 ns in the present example.

In general, more than two channels, e.g. four, six, eight, etc. can also belong to a group; in each case, it would be, for example, bits b7 of the channels of one group which would be transmitted, then bits b6, and so forth. In addition, the invention is not restricted to one octet being transmitted in each case; instead, a data ~~multiplet~~ time slot formed of n bits can just as well be allocated to each channel where n can assume any values from 4, e.g. n = 4, 6, 10 or 16. Also, instead of a binary coding of the data bits, a ~~multiplet~~ time slot of digital data coded in a non-binary form, e.g. characters coded via predetermined discrete levels, can be used in the ~~multiplets~~ time slots.

Due to this time-interleaved transmission of the bits of a group, the transmitting and receiving parts only need to generate or, respectively, receive each second bit - or, respectively, each fourth, sixth, eighth, etc. bit in dependence on the number of channels in a group - of the frame TFR transmitted with the signal ~~bp~~ pb. This results in a data processing rate which is reduced compared with the data rate of the PCM bus for the SLM card. Each SLM card can thus operate at a lower clock rate. It is possible to use, e.g. the

"fast" clock ck8 through the use of a suitably selected clock division for this purpose.

Please replace the paragraph beginning on page 31, line 17 and ending on page 32, line 4 with the following amended paragraph:

As already mentioned, the invention is not restricted to the case where the data ~~multiplets~~ time slots of in each case two channels are transmitted interleaved with one another in a group. Instead, this can also be performed for, e.g., four or more channels. If, for example starting with the example shown in Fig. 1, four channels per group are transmitted - that is to say first bit 7 of channels CHA, CHB, CHC, CHD, then bit 6 of these channels and so forth, that is to say a total of 4 x 8 = 32 bits per group - the required processing speed in the central components would be reduced to one half as a result, the data rate of the central bus system remaining the same, and similarly that for weighting bit collisions on the collision detection bus would be almost doubled correspondingly.